1   1.   A method comprising:

2   detecting that a processor's frequency has

3   changed in response to processor cooling; and

4   generating an interrupt in response to the

5   detection of the frequency change.

1   2.   The method of claim 1 including providing an

2   interrupt to an operating system.

1   3.   The method of claim 1 including reading the

2   performance state of the processor in response to the

3   interrupt.

1   4.   The method of claim 3 including determining a new

2   performance state.

1   5.   The method of claim 4 including scheduling a

2   bandwidth allocation.

1   6.   The method of claim 2 including setting up a

2   periodic timer.

1   7.   The method of claim 6 including monitoring the

2   processor temperature at periodic intervals.

1   8.   The method of claim 1 including detecting a high

2   temperature or a low temperature interrupt and reading the

3   processor performance state in response to the detection of

4   a high temperature or a low temperature interrupt.

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1   9.   The method of claim 1 wherein detecting a

2 frequency change includes detecting a processor phase

3 locked loop event.

1   10.   The method of claim 1 including using hardware

2 controlled throttling.

1   11.   An article comprising a medium storing ·

2 instructions to enable a processor-based system to:

3   detect that a processor's frequency has changed

4 in response to processor cooling; and

5   generate an interrupt in response to the

6 detection of the frequency change.

1   12.   The article of claim 11 further storing

2 instructions to enable a processor-based system to provide

3 an interrupt to an operating system.

1   13.   The article of claim 11 further storing

2 instructions to enable a processor-based system to read the

3 performance state of the processor in response to the

4 interrupt.

1   14.   The article of claim 13 further storing

2 instructions to enable a processor-based system to

3 determine a new performance state.

1   15. The article of claim 14 further storing

2 instructions to enable a processor-based system to schedule

3 a bandwidth allocation.

1   16. The article of claim 12 further storing

2 instructions to enable a processor-based system to set up a

3 periodic timer.

1   17. The article of claim 16 further storing

2 instructions to enable a processor-based system to monitor

3 the processor temperature at periodic intervals.

1   18. The article of claim 11 further storing

2 instructions to enable a processor-based system to detect a

3 high temperature or a low temperature interrupt and read

4 the processor performance state in response to the

5 detection of a high temperature or a low temperature

6 interrupt.

1   19. The article of claim 11 further storing

2 instructions to enable a processor-based system to detect a

3 processor phase locked loop event.

1   20. The article of claim 11 further storing

2 instructions to enable a processor-based system to use

3 hardware controlled throttling.

1   21. A system comprising:

2   a processor;

3   a temperature sensor coupled to said processor;

4   and

5   a storage storing instructions that enable the

6   processor to detect that the processor's frequency has

7   changed in response to processor cooling and generate an

8   interrupt in response to detection of the frequency change.

1   22. The system of claim 21 including a storage

2   storing an operating system, said interrupt being provided

3   to the operating system.

1   23. The system of claim 21 wherein said storage

2   stores instructions that enable the processor to read the

3   performance state of the processor in response to an

4   interrupt.

1   24. The system of claim 21 wherein said processor

2   determines a new performance state.

1   25. The system of claim 24 wherein said storage

2   stores instructions that enable the processor to schedule a

3   bandwidth allocation.

1   26. The system of claim 22 wherein said storage

2   stores instructions that enable the processor to set up a

3   periodic timer.

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1   27.   The system of claim 26 wherein said storage
2 stores instructions that enable the processor to monitor
3 the processor temperature at periodic intervals.

1   28.   The system of claim 21 wherein said storage
2 stores instructions that enable the processor to detect a
3 high temperature or a low temperature interrupt and read
4 the processor performance state in response to the
5 detection of a high temperature or a low temperature
6 interrupt.

1   29.   The system of claim 21 wherein said storage
2 stores instructions that enable the processor to detect a
3 processor phase locked loop event.

1   30.   The system of claim 21 including hardware
2 controlled throttling.